SAA7173HL

Audio and video broadcast decoder

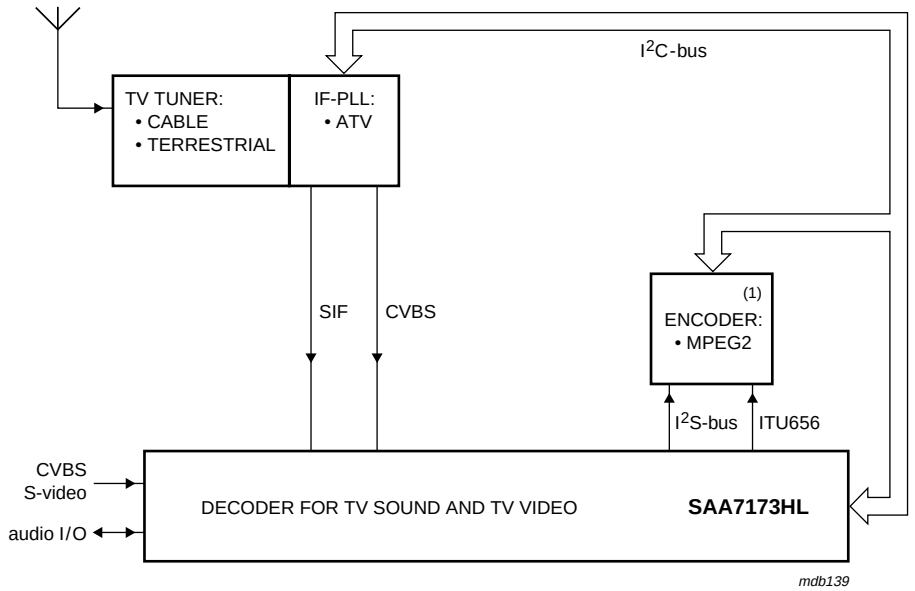
Rev. 01 — 11 May 2005 Product data sheet

1. General description

The audio and video broadcast decoder SAA7173HL is a highly integrated, low cost and solid foundation for analog TV.

The analog video is sampled by 9-bit ADCs, decoded by a multi-line adaptive comb filter and scaled horizontally, vertically and by field rate. Multiple video output formats are available: 8-bit serial or 16-bit parallel (YUV), gamma-compensated or black-stretched.

Analog TV sound is digitized and stereo decoded (BTSC and EIAJ). Audio is digitized I^2S-bus and baseband audio left/right signal.



(1) Alternative.

Fig 1. Application diagram for capturing live TV video and audio streams and MPEG encoding

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2. Features

2.1 TV video decoder and video scaling

- All-standards TV decoder: NTSC, PAL and SECAM
- Five analog video inputs: CVBS and S-video
- Video digitizing by two 9-bit ADCs at 27 MHz
- Sampling according to *ITU-R BT.601* with 720 pixels/line
- Adaptive comb filter for NTSC and PAL, also operating for non-standard signals
- Automatic TV standard detection
- Three-level Macrovision copy protection detection according to Macrovision detect specification Rev.1
- Control of brightness, contrast, saturation and hue
- Versatile filter bandwidth selection
- Horizontal and vertical downscaling or zoom
- Adaptive anti-alias filtering
- Capture of raw VBI samples
- Two alternating settings for active video scaling, e.g. for independent capturing and preview definition
- Output in YUV
- Gamma compensation, black stretching.

2.2 TV sound decoder and TV audio I/O

- BTSC and EIAJ TV sound decoder
- dbx-TV Noise Reduction decoding for BTSC systems
- FM radio stereo decoding
- Input of analog SIF signal and 8-bit ADC at 24.576 MHz
- Automatic sound standard detection
- Automatic dematrixing (stereo, dual)
- Volume, balance, bass and treble control
- Automatic Volume Levelling (AVL)
- Incredible Mono, Incredible Stereo
- Audio sampling clock can be locked to video frame rate (no drift of audio stream against video stream)
- Four analog audio baseband inputs (two stereo pairs) and on-chip stereo ADCs
- Supported audio sampling rates: 32 kHz, 44.1 kHz and 48 kHz
- Input of external audio reference clock, e.g. 24.576 MHz
- Output of audio master clock ($768 \times f_s$, $512 \times f_s$, $384 \times f_s$ or $256 \times f_s$ selectable).

2.3 Peripheral interface

- I^2C-bus slave interface: 3.3 V and 5 V compatible, 100 kHz and 400 kHz mode
- Digital video output: ITU, VIP, VMI and ZV formats
- Two digital audio outputs: I^2S-bus for up to 4 channels
- Analog stereo audio output
- Integrated analog audio pass-through

- Propagate reset
- General purpose I/O, e.g. for strapping and interrupt.

3. Applications

3.1 Innovation

- Manufacturing more cost efficient products with higher capability, e.g.:
  - Integration of high-quality multi-standard analog TV decoding
  - Integration of high-quality sound experiences
  - Fast input-switching in surveillance applications.

3.2 Products

- Terrestrial TV
- Cable TV
- Satellite set-top box
- Hybrid TVs (analog and digital TV)
- Desktop PC
- Portable PC
- USB/1394 video dongle
- VCRs with fast search, shuttle and freeze-frame functionality
- Personal Video Recorder (PVR) with time shifting
- DVD recorder
- and more.

4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3.0	3.3	3.6	V
P_{tot}	total power dissipation		-	1.35	1.6	W
P_{stb}	standby power dissipation		-	0.2	-	W
T_{amb}	ambient temperature		0	-	70	°C

5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
SAA7173HL	LQFP128	plastic low profile quad flat package; 128 leads; body 14 × 20 × 1.4 mm	SOT425-1

6. Block diagram

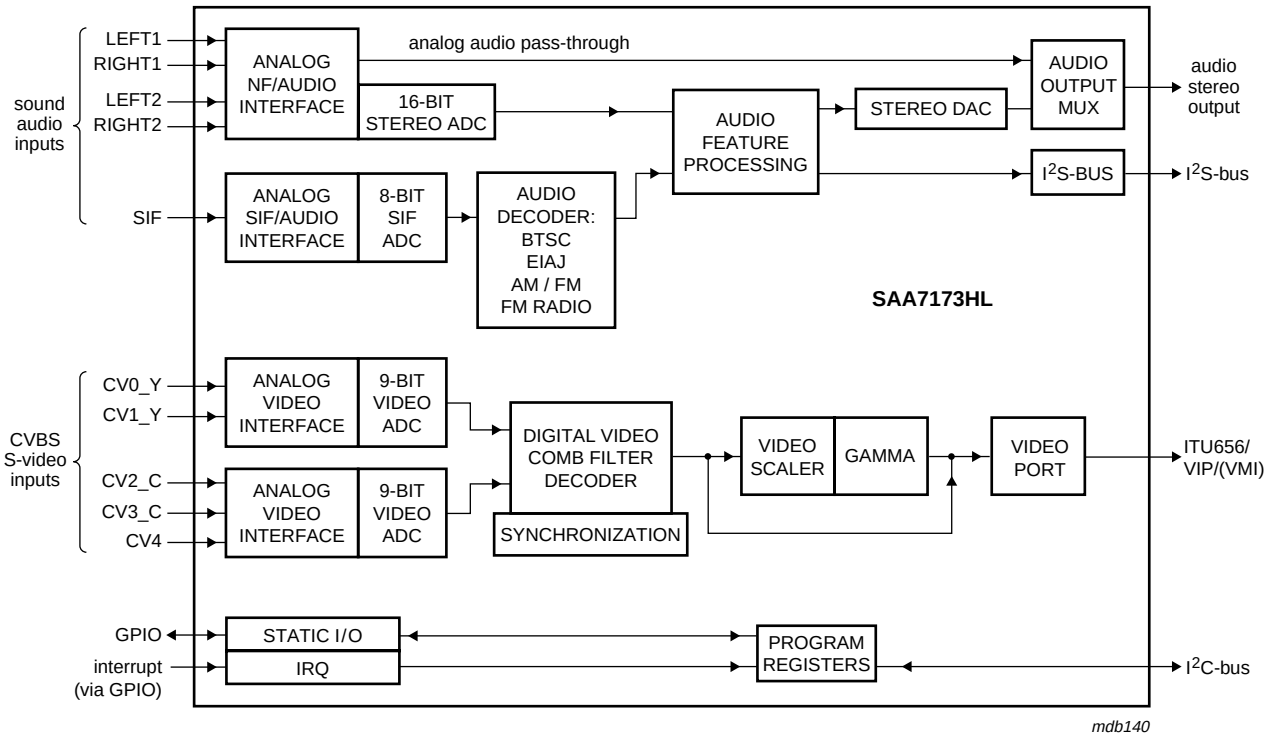


Fig 2. Block diagram

7. Pinning information

7.1 Pinning

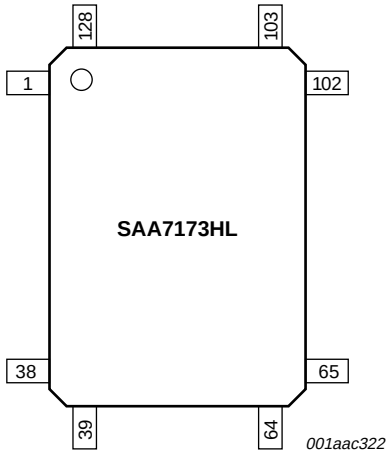


Fig 3. Pin configuration

Table 3: Pin allocation table

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{DDD}	33	TEST29	65	V_{DDD}	97	V_{SSA}
2	TEST1	34	TEST30	66	V_CLK	98	RIGHT1
3	TEST2	35	TEST31	67	GPIO17	99	V_{REF0}
4	TEST3	36	TEST32	68	GPIO16	100	RIGHT2
5	TEST4	37	TEST33	69	GPIO15	101	V_{REF1}
6	TEST5	38	V_{DDD}	70	GPIO14	102	V_{REF2}
7	TEST6	39	V_{SSD}	71	GPIO13	103	OUT_RIGHT
8	TEST7	40	TEST34	72	GPIO12	104	OUT_LEFT
9	TEST8	41	TEST35	73	V_{DDD}	105	PROP_RST_N
10	TEST9	42	TEST36	74	V_{SSD}	106	SIF
11	TEST10	43	TEST37	75	GPIO11	107	V_{REF3}
12	TEST11	44	TEST38	76	GPIO10	108	V_{SSA}
13	TEST12	45	TEST39	77	GPIO9	109	CV2_C
14	TEST13	46	TEST40	78	GPIO8	110	V_{DDA}
15	TEST14	47	TEST41	79	GPIO7	111	V_{REF4}
16	TEST15	48	TEST42	80	GPIO6	112	DRCV_Y
17	TEST16	49	TEST43	81	GPIO5	113	V_{SSA}
18	TEST17	50	TEST44	82	GPIO4	114	CV0_Y
19	V_{DDD}	51	TEST45	83	GPIO3	115	V_{DDA}
20	V_{SSD}	52	TEST46	84	GPIO2	116	CV1_Y
21	TEST18	53	TEST47	85	GPIO1	117	DRCV_C
22	TEST19	54	V_{DDD}	86	GPIO0	118	CV3_C
23	TEST20	55	V_{SSD}	87	GPIO27	119	V_{SSA}
24	TEST21	56	GPIO23	88	GPIO26	120	CV4
25	n.c.	57	GPIO22	89	GPIO25	121	TRST_N
26	TEST22	58	GPIO21	90	SCL	122	TCK
27	TEST23	59	GPIO20	91	SDA	123	TMS
28	TEST24	60	GPIO19	92	V_{DDD}	124	TDO
29	TEST25	61	GPIO18	93	V_{SSD}	125	TDI
30	TEST26	62	XTALI	94	LEFT2	126	INT
31	TEST27	63	XTALO	95	V_{DDA}	127	I2C_RST
32	TEST28	64	V_{SSD}	96	LEFT1	128	V_{SSD}

7.2 Pin description

The SAA7173HL is packaged in a rectangular plastic low profile quad flat package with 128 pins (LQFP128); see Figure 3.

Table 4: Pin description overview

Pin category	Table number
Power supply pins	Table 5
Analog interface pins	Table 6
I^2C-bus interface pins	Table 7
General purpose interface (GPIO) pins and functions	Table 8
Test pins and not connected pins	Table 9
Joint Test Action Group (JTAG) test interface pins (for boundary scan test)	Table 10

Table 5: Power supply pins

Symbol	Pin	Type [1]	Description
V_{SSD}	20, 39, 55, 64, 74, 93 and 128	VG	digital ground for digital circuit, core and I/Os
V_{DDD}	1, 19, 38, 54, 65, 73 and 92	VS	digital supply voltage for digital circuit, core and I/Os
V_{SSA}	97, 108, 113 and 119	AG	analog ground for integrated analog signal processing
V_{DDA}	95, 110 and 115	AS	analog supply voltage for integrated analog signal processing

[1] The pin types are defined in Table 11.

Table 6: Analog interface pins; the SAA7173HL offers an interface for analog video and audio signals

Symbol	Pin	Type [1]	Description
Audio and video interface; the related analog supply pins are included			
XTALI	62	CI	quartz oscillator input: 24.576 MHz
XTALO	63	CO	quartz oscillator output
LEFT2	94	AI	analog audio stereo left 2 input or mono input
V_{DDA}	95	AS	analog supply voltage (3.3 V)
LEFT1	96	AI	analog audio stereo left 1 input or mono input; default analog pass-through to pin OUT_LEFT after reset
V_{SSA}	97	AG	analog ground (for audio)
RIGHT1	98	AI	analog audio stereo right 1 input or mono input; default analog pass-through to pin OUT_RIGHT after reset
V_{REF0}	99	AR	analog reference ground for audio Sigma Delta ADC; to be connected to V_{SSA}
RIGHT2	100	AI	analog audio stereo right 2 input or mono input
V_{REF1}	101	AR	analog reference voltage for audio Sigma Delta ADC; to be connected to V_{DDA} and via a 220 nF capacitor connected to pin V_{REF0}
V_{REF2}	102	AR	analog reference voltage for audio Sigma Delta ADC; to be supported with two parallel capacitors of 47 µF and 0.1 µF connected to V_{SSA}
OUT_RIGHT	103	AO	analog audio stereo right channel output; 1 V (RMS) line-out, coupling capacitor of 2.2 µF
OUT_LEFT	104	AO	analog audio stereo left channel output; 1 V (RMS) line-out, coupling capacitor of 2.2 µF

Table 6: Analog interface pins; the SAA7173HL offers an interface for analog video and audio signals *...continued*

Symbol	Pin	Type [1]	Description
PROP_RST_N	105	AO	analog output for test and debug purposes
SIF	106	AI	sound IF input from TV tuner (4.5 MHz to 9.2 MHz); coupling capacitor of 47 pF after the termination with 50 Ω
V_{REF3}	107	AR	analog reference voltage for audio FIR-DAC and SCART audio input buffer; to be supported with two parallel capacitors of 47 µF and 0.1 µF connected to V_{SSA}
V_{SSA}	108	AG	analog ground
CV2_C	109	AI	composite video input (mode 2) or C input (modes 6 and 8)
V_{DDA}	110	AS	analog supply voltage (3.3 V)
V_{REF4}	111	AR	analog reference voltage; to be supported with a capacitor of 220 nF connected to V_{SSA}
DRCV_Y	112	AR	differential reference connection (for CV0 and CV1); to be supported with a capacitor of 47 nF connected to V_{SSA}
V_{SSA}	113	AG	analog ground
CV0_Y	114	AI	composite video input (mode 0) or Y input (modes 6 and 8)
V_{DDA}	115	AS	analog supply voltage (3.3 V)
CV1_Y	116	AI	composite video input (mode 1) or Y input (modes 7 and 9)
DRCV_C	117	AR	differential reference connection (for CV2, CV3 and CV4); to be supported with a capacitor of 47 nF connected to V_{SSA}
CV3_C	118	AI	composite video input (mode 3) or C input (modes 7 and 9)
V_{SSA}	119	AG	analog ground
CV4	120	AI	composite video input (mode 4)

[1] The pin types are defined in Table 11.

Table 7: I^2C-bus interface

Symbol	Pin	Type [1]	Description
SCL	90	IO2	serial clock input
SDA	91	IO2	serial data input and output; always available
PROP_RST_N	105	GO	propagate reset output; to peripheral board circuitry (active LOW)
INT	126	O	interrupt output (open-drain)
I2C_RST	127	I	I^2C-bus reset input; the falling edge of the HIGH pulse resets the device; set to LOW during power-up and at normal operation

[1] The pin types are defined in Table 11.

Table 8: GPIO pins and functions [1]

Symbol	Pin	Type [2]	Audio and video port outputs	GPIO
GPIO23	56	GIO	HSYNC	R/W, INT
GPIO22	57	GIO	VSYNC	R/W, INT
GPIO21 to GPIO19	58 to 60	GIO	-	R/W
GPIO18	61	GIO	VAUX2; A_CLK_master, A_REF_CLK	R/W, INT
V_CLK	66	GO	V_CLK (also gated)	-
GPIO17	67	GIO	VAUX1 (e.g. VACTIVE); A_SDO_aux, I^2S-bus 2 data	R/W
GPIO16	68	GIO	-	R/W, INT
GPIO15 to GPIO12 and GPIO11 to GPIO8	69 to 72 and 75 to 78	GIO	VP[7:0] for formats: *ITU-R BT.656*, VMI, VIP (1.1, 2.0), etc.	R/W
GPIO7 to GPIO0	79 to 86	GIO	VP extension for 16-bit formats: ZV, VIP-2, DMSD, etc.	R/W
GPIO27	87	GIO	A_SDO (I^2S-bus 1 data)	R/W
GPIO26	88	GIO	A_WS (I^2S-bus word select)	R/W
GPIO25	89	GIO	A_SCK (I^2S-bus clock)	R/W

[1] The SAA7173HL offers a peripheral interface with General Purpose Input/Output (GPIO) pins. Dedicated functions can be selected:

a) Digital Video Port (VP): output only; in 8-bit and 16-bit formats, such as VMI, DMSD (*ITU-R BT.601*); zoom-video, with discrete sync signals; *ITU-R BT.656*; VIP (1.1 and 2.0), with sync encoded in SAV and EAV codes.

b) GPIO: as default (no other function selected); static (no clock); read and write from or to individually selectable pins; latching 'strap' information at system reset time.

c) Use an external pull-up resistor of 4.7 kΩ at GPIO16 for an external 24.576 MHz crystal; due to an internal pull-down resistor an open GPIO16 pin requires an external 32.11 MHz crystal.

[2] The pin types are defined in Table 11.

Table 9: Test and not connected pins

Symbol	Pin	Type [1]	Description
TEST1 and TEST22 to TEST25	2 and 26 to 29	-	recommended to connect to V_{DD}, or do not connect
TEST2 to TEST17, TEST18 to TEST21, TEST26 to TEST33 and TEST35 to TEST47	3 to 18, 21 to 24, 30 to 37 and 41 to 53	-	do not connect
TEST34	40	-	connect to ground
n.c.	25	-	not connected

[1] The pin types are defined in Table 11.

Table 10: JTAG test interface pins

Symbol	Pin	Type [1]	Description
TRST_N	121	I	test reset input: drive LOW for normal operating (active LOW)
TCK	122	I	test clock input: drive LOW for normal operating
TMS	123	I	test mode select input: tie HIGH or let float for normal operating
TDO	124	O	test serial data output: 3-state
TDI	125	I	test serial data input: tie HIGH or let float for normal operating

[1] The pin types are defined in Table 11.

Table 11: Pin type description

Type	Description
AG	analog ground
AI	analog input; video, audio and sound
AO	analog output
AR	analog reference support pin
AS	analog supply voltage (3.3 V)
CI	CMOS input; 3.3 V signal level (not 5 V tolerant)
CO	CMOS output; 3.3 V signal level (not 5 V tolerant)
GIO	digital input/output (GPIO); 3.3 V signal level (5 V tolerant)
GO	digital output (GPIO); 3.3 V signal level (5 V tolerant)
I	JTAG test input for I^2C-bus reset
IO2	digital input and output of the I^2C-bus interface; 3.3 V and 5 V compatible; auto-adapting
O	JTAG test output or interrupt output
VG	ground for digital supply
VS	supply voltage (3.3 V)

8. Limiting values

Table 12: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All ground pins connected together and grounded (0 V); all supply pins connected together.

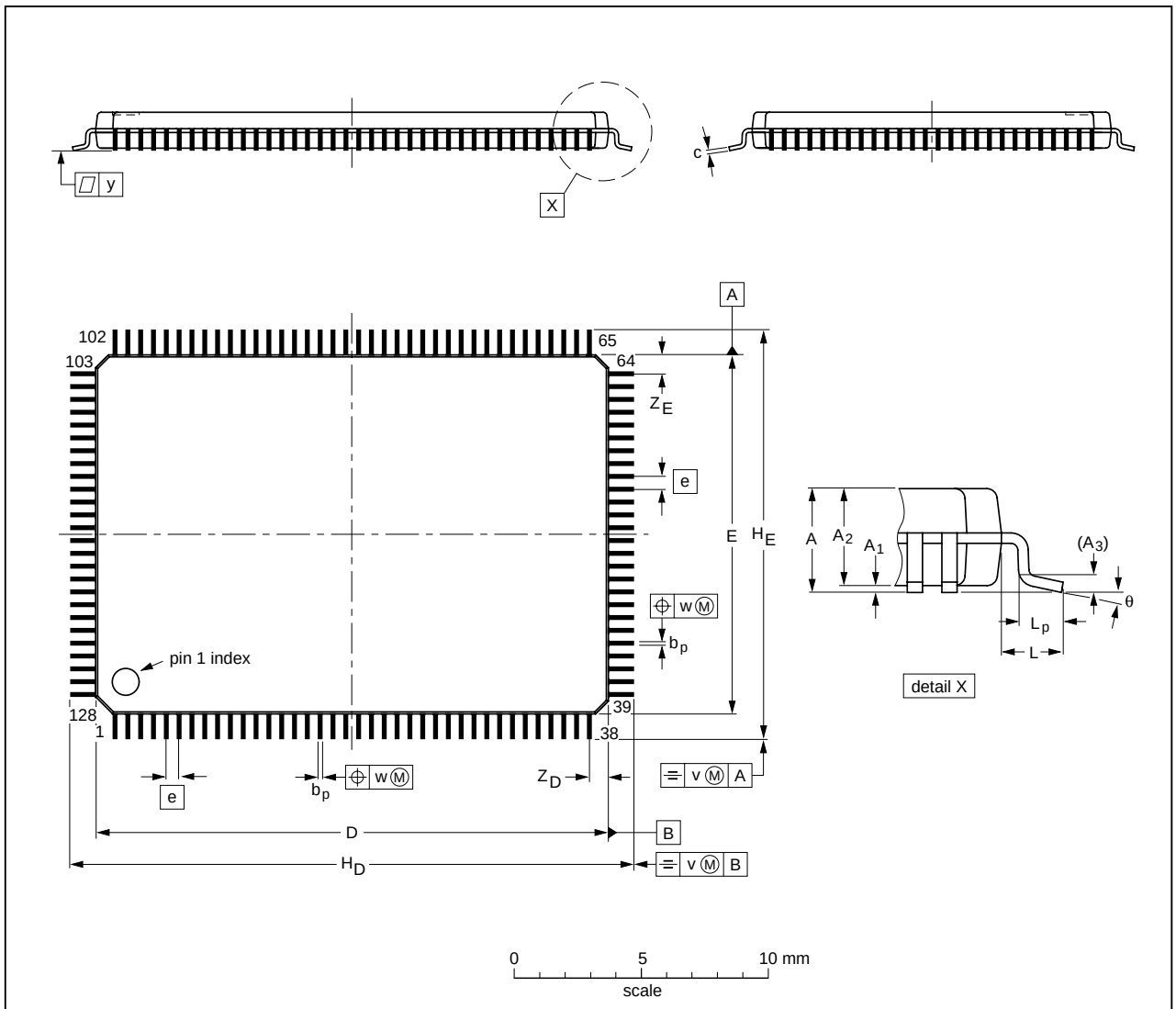
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDD}	digital supply voltage			–0.5	+4.6	V
V_{DDA}	analog supply voltage			–0.5	+4.6	V
ΔV_{SS}	voltage difference between pins V_{SSA} and V_{SSD}			-	100	mV
V_{IA}	input voltage at analog inputs			–0.5	+4.6	V
$V_{I(in)}$	input voltage at pins XTALI, SDA and SCL			–0.5	V_{DDD} + 0.5	V
V_{ID}	input voltage at digital I/O stages	outputs in 3-state				
		$-0.5 < V_{DDD} < +3.0$ V		–0.5	+4.6	V
		$-0.5 < V_{DDD} < +3.6$ V		–0.5	+5.5	V
T_{stg}	storage temperature			–65	+150	°C
T_{amb}	ambient temperature			0	70	°C
V_{esd}	electrostatic discharge voltage	human body model	[1]	-	±2000	V
		machine model	[2]	-	±150	V

[1] Class 2 according to EIA/JESD22-A114-B.

[2] Class A according to EIA/JESD22-A115-A.

9. Package outline

LQFP128: plastic low profile quad flat package; 128 leads; body 14 x 20 x 1.4 mm **SOT425-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	14.1 13.9	0.5	22.15 21.85	16.15 15.85	1	0.75 0.45	0.2	0.12	0.1	0.81 0.59	0.81 0.59	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT425-1	136E28	MS-026				~~00-01-19~~ 03-02-20

Fig 4. Package outline SOT425-1 (LQFP128)

10. Revision history

Table 13: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
SAA7173HL_SDS_1	20050511	Product data sheet	-	9397 750 14564	-

11. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

12. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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16. Contents

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